REMARKS

An excess claim fee payment letter is submitted herewith for two (2) additional independent claims and two (2) additional total claims.

Claims 1-22 are all the claims presently pending in the application. Claims 1, 3, and 6-10 are amended to more clearly define the invention and claims 11-22 are added. Claims 1, 3, 7, 11, and 17 are independent.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicant also notes that, notwithstanding any claim amendments herein or later during prosecution, Applicant's intent is to encompass equivalents of all claim elements.

Applicant gratefully acknowledges that claims 3-10 are allowed. However, Applicant respectfully submits that all of the claims are allowable.

Applicant gratefully acknowledges that claim 2 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, Applicant respectfully submits that all of the claims are allowable.

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by the Davis reference.

This rejection is respectfully traversed in the following discussion.

I. THE INFORMATION DISCLOSURE STATEMENT

The Examiner indicated that the Information Disclosure Statement that was filed on February 5, 2004, did not include legible copies of France 2817970, the European Search

Report dated January 14, 2004, and "Voltage comparator circuit, IBM Vol. No. 4, Sept. 1974, pp 1151 - 1152. In particular, the Examiner notes that these references "are missing from the application."

Applicant encloses a re-submission of the February 5, 2004, Information Disclosure Statement including the references that the Examiner is missing from his file and another form PTO-1449 for the Examiner's convenience.

Applicant respectfully requests that the Examiner indicate consideration of all references that were submitted in the Information Disclosure Statement that was filed on February 5, 2004.

II. THE CLAIMED INVENTION

An exemplary embodiment of the claimed invention, as defined by independent claim 1, for example, is directed to a device for setting a hysteresis characteristic with respect to an input signal. The device includes a voltage dividing circuit for dividing a voltage of the input signal into a first voltage and a second voltage which is lower than the first voltage, and a computer. The computer includes a first port to which the first voltage is given, and a second port to which the second voltage is given. The computer performs a predetermined software process to set a hysteresis characteristic. The process includes, when the voltages given to the first and second ports are equal to or higher than a predetermined threshold, determining the input signal to have a high level, when the voltage given to the first port is equal to or higher than the threshold and the voltage given to said second port is lower than the threshold, making a same determination as an immediately preceding determination, and when the voltages given to the first and second ports are lower than the predetermined threshold,

determining the input signal to have a low level.

Conventional hysteresis characteristic setting circuits include a logic circuit or a comparator circuit that uses a Schmitt trigger that includes operational amplifiers or transistors and resistors. Thus, these conventional circuits have a large number of components, which increases production costs and requires a large installation space.

In stark contrast, the present invention provides a hysteresis characteristic setting circuit that includes a computer, which when voltages given to first and second ports are equal to or higher than a predetermined threshold, determining the input signal to have a high level, when the voltage given to the first port is equal to or higher than the threshold and the voltage given to said second port is lower than the threshold, making a same determination as an immediately preceding determination, and when the voltages given to the first and second ports are lower than the predetermined threshold, determining the input signal to have a low level. In this manner, the present invention provides a hysteresis characteristic setting circuit that includes fewer components than the conventional hysteresis characteristic setting circuits. (Page 3, lines 8-12).

III. THE PRIOR ART REJECTION

The Examiner alleges that the Davis reference teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by the Davis reference.

The Examiner's alleged significance of the Davis reference is murky, at best, as the Office Action did not explain the pertinence of this reference to the specific elements which are recited by the claims being rejected, as required by M.P.E.P. § 707.5.

Note that MPEP 707.05 states:

"During the examination of an application or reexamination of a patent, the examiner should cite appropriate prior art which is nearest to the subject matter defined in the claims. When such prior art is cited, its pertinence should be explained." (Emphasis added).

The Examiner's rejection also fails to comply with 37 C.F.R. §1.104(c)(2) which requires that "the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified." (Emphasis added).

In this case, not only has the Examiner failed to cite the particular portion of the Davis reference which may have been relied upon, but the Examiner has also failed to clearly explain the pertinence of the Davis reference to each rejected claim.

Taking only a single example from the Office Action, the Examiner refers to Figure 3 and the outputs Q9 and Q14 from binary counter 40 and appears to allege that these outputs correspond to "a voltage dividing circuit for dividing a voltage said (sic) input signal into a first voltage and a second voltage which is lower than said first voltage."

However, it is not apparent as to which portion of the Davis reference that is disclosed by Figure 3 that the Examiner alleges corresponds to "a voltage dividing circuit for dividing a voltage said (sic) input signal into a first voltage and a second voltage which is lower than said first voltage."

Figure 3 of the Davis reference discloses two voltage dividers. The first voltage divider includes resistors R7 and R8 (col. 9, line 59) and the second voltage divider includes

resistors R3, R4, and R6 (col. 10, line 8). The Examiner does not indicate with particularity which of these voltage dividers correspond to the claimed voltage divider.

Further, surely the Examiner is not alleging that the outputs Q9 and Q14 from binary counter 40 correspond to the claimed voltage divider.

Moreover, even if the Examiner is able to point to a voltage divider in the system that is disclosed by the Davis reference, there is no teaching or suggestion in the Davis reference of setting the hysteresis as clearly recited by the independent claims.

The Examiner merely keeps repeating "unit p1, p2," but it is clear that these two ports merely receive the inputs and do not themselves "set" anything at all, let alone teach or suggest setting a hysteresis characteristic as recited by the plain meaning of the language in the independent claims.

The Office Action further does not make clear what the Examiner alleges corresponds to the outputs Q9 and Q14 from binary counter 40. The Office Action does not make clear whether the Examiner alleges that the outputs Q9 and Q14 from binary counter 40 correspond to the claimed voltage dividing circuit, a source for an input signal (i.e. first voltage), or a source for a second voltage.

Indeed, the Examiner does not even make clear which of the several signals that are disclosed by the Davis reference that the Examiner alleges corresponds to the claimed input signal.

To assist Applicant's understanding, Applicant hereby respectfully requests that the Examiner comply with the requirements of M.P.E.P. § 707.5 by explaining in detail the correspondence between the specific features recited by claim 1 and the particular portions of the Davis reference.

Further, in view of the murkiness of the Examiner's rejection, Applicant respectfully submits that the Examiner cannot make the next Office Action final due to lack of any adequate explanation of how the Examiner alleges the Davis reference discloses the features of claim 1. Applicant cannot reasonably be asked to decipher a rejection that does not clarify the particular portions of a reference, which corresponds to the specific features of a rejected claim.

To further the prosecution of this application, however, Applicant has closely reviewed the Davis reference to address the clear differences between the Davis reference and the claims.

The Davis reference does not teach or suggest the features of the claimed invention including a computer, which when voltages given to first and second ports are equal to or higher than a predetermined threshold, determining the input signal to have a high level, when the voltage given to the first port is equal to or higher than the threshold and the voltage given to said second port is lower than the threshold, making a same determination as an immediately preceding determination, and when the voltages given to the first and second ports are lower than the predetermined threshold, determining the input signal to have a low level. In this manner, the present invention provides a hysteresis characteristic setting circuit that includes fewer components than the conventional hysteresis characteristic setting circuits.

Indeed, Applicant respectfully submits that the method and apparatus for initializing a microprocessor to insure fault-free operation as disclosed by the Davis reference has absolutely nothing to do with setting a hysteresis characteristic, let alone a device for setting a hysteresis characteristic that includes a computer, which when voltages given to first and second ports are equal to or higher than a predetermined threshold, determining the input

signal to have a high level, when the voltage given to the first port is equal to or higher than the threshold and the voltage given to said second port is lower than the threshold, making a same determination as an immediately preceding determination, and when the voltages given to the first and second ports are lower than the predetermined threshold, determining the input signal to have a low level.

The Examiner cites Figure 3 of the Davis reference which discloses a binary counter 40 connected to a microprocessor 15 via initialization means 26. (Col. 8, lines 39-44).

The Davis reference further explains the operation of the method and apparatus for initializing a microprocessor to insure fault-free operation in further detail with reference to Figures 3-4, 5A, and 5B.

A first timer means (11 from Figure 2) may be implemented internally in the microprocessor 15, in which instance the microprocessor would output a notice signal on notice port P2 to send a warning of impending initialization (col. 11, lines 27 - 43). Alternatively, the first timer means (11 from Figure 2) may be implemented using an external hardware counter such as the binary counter 40 which "output Q9 set at TTL low level and the output Q14 set at a TTL high level, the port P2 is pulled to a TTL high level via the coupling resistor R5, thereby sending a notice signal at time t1 to the microprocessor 15.

"In response to the notice signal, the microprocessor 15 operates to complete current operating tasks and to store selected critical operating data prior to the initialization of the microprocessor 15 . . . . After completing the current operating tasks and storing selected critical operating data, the microprocessor toggles the port P1 to a TTL high level at time t2 to indicate that the microprocessor 15 is ready for initialization." (Col. 11, line 58 - col. 12, line 3, see also Figure 4).

"When the port P1 is set to a TTL high level at time t2, the voltage divider defined by the resistors R3, R4, and R6 sets a voltage of 2/3 Vs at the terminal A. Because the voltage at terminal A is now greater than the threshold voltage of ½ Vs at the terminal B, each of the comparators 41 and 42 changes operating states and outputs a reset signal." (Col. 12, lines 4 - 18).

Clearly, the Davis reference does not teach or suggest a hysteresis characteristic, let alone a device for setting a hysteresis characteristic that includes a computer, which when voltages given to first and second ports are equal to or higher than a predetermined threshold, determining the input signal to have a high level, when the voltage given to the first port is equal to or higher than the threshold and the voltage given to said second port is lower than the threshold, making a same determination as an immediately preceding determination, and when the voltages given to the first and second ports are lower than the predetermined threshold, determining the input signal to have a low level.

Therefore, the Davis reference does not teach or suggest each and every element of the claimed invention and the Examiner is respectfully requested to withdraw this rejection of claim 1.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-22, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 4/18/05

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